An algorithm of defects inspection based on a chip image and methods of edge detection and binary image histogram

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ABSTRACT: It's inevitable that defect occurs for a few of chips during manufacture. Unqualified chips with defect size of impacting chip quality have to be discarded. But present chip defect inspection system is designed using frame CCD imagers. Some drawbacks exist for this system, such as pause image acquisition, complicate and time-consuming image processing and mosaic, etc. Efficiency and accuracy of defect inspection degrade substantially. So chip defect is now still inspected manually in factories. Therefore, a chip defect inspection system to inspect defects automatically is demanded.

Here we address a novel algorithm to precisely identify defects with the size of greater than criterion based on a chip raw image. Characteristics of proposed inspection system are also introduced. Schneider lens with good optical performance is adopted, so image radiometric and geometric calibration can be neglected. It's very important and critical for proposed algorithm to identify chip defects in real-time. Proposed algorithm is composed of 2 parts: (1) deriving the region of interest (chip) from raw image, and (2) inspecting the defects on chips. ROI derivation includes procedures of edge detection on raw image, chip boundary designation, four corners derivation for chip, parameters derivation of Affine transformation, and image segmentation. Chip edge (binarized) image is derived to achieve the high correctness of defect inspection. Defect inspection comprises procedures of calculating the pixels value difference on chip edge image with defect template within a scan window, and comparing this difference with criterion to check the quality of inspected chips. Thus, proposed algorithm has advantages of calculation with simplicity, and capability to identify the size and type of defects. And efficiency and accuracy of defect inspection will be improved substantially. Moreover, inspection system can be operated automatically during sorting process.

1. Introduction

Defects exist for a few of chips during their manufacturing. Unqualified chips with defect size of greatre than the criterion of impacting chip quality have to be inspected and removed during packing process. Therefore, chips defect is mostly inspected manually now. Manual inspection induces some issues such as inconsistent inspection criterion, unstable quality of chips and low throughput.

Inspection systems for chip defects have been developed to solve problems mentioned above. But existent inspection systems are designed based on frame CCD imagers. Therefore, some imperfections exist for these systems, such as pause type of image acquisition, higher possibility of malfunction for moving parts, necessity of image radiometric and geometric calibration for acquired frame images per chip and then pieced them together into long mosaic one before inspection for chips with longer size, etc. Thus, efficiency and accuracy of inspection degrade signaficantly. Consequently, chips defect is still inspected manually on production lines.

In this article, we address a Chip Defect Inspection System (CDIS) based on a line scan imager, and a novel algorithm for image processing and chip defects inspection is presented.

2. System Architecture and Characteristics

2.1 System Analysis and Design

According to the inspection requirements for chips defect on chip sorter, an automatic inspection system is developed to check defects out from the back side of chips directly. The system requirements are described as follows: (1) Size range of inspected chips is between 0.5 x 0.5 ~ 2.0 x 40 mm, (2) Read on fly capability and the moving speed of inspected chips shall be greater than 0.6 m/sec, (3) Defects with size of greater than 15 μm shall be inspected.

Based on above system requirements and drawbacks of existent systems, and considering system performance, available sources and cost, the specifications of opto-mechanical apparatus (OMA) are listed as follows:

(1) Objects spatial resolution of 5μm for inspection system,
(2) Magnification of 2 for optical lens is selected,
(3) Image line rate of line scan imager shall be greater than 120 kHz,
(4) Data rate of image acquisition shall be greater than 500 Mbytes/sec.

According to results of system analysis and specifications of opto-mechanical apparatus, we design an inspection system for chip defects inspection based on a line scan imager and a novel scheme of defects inspection. CDIS comprises following subsystems: (1) Line Image Acquisition (LIA) for line image acquisition and storage with high performance, (2) Illumination & Environment Control (IEC) for light configuration and control in the image acquisition region to enhance the contrast of image, (3) Defects Inspection (DI) for acqusition sync control and image receiving from LIA, image processing for ROI extraction and chip defect inspection, (4) Operations & Management (O&M) for system operations and management, and graphic user interfaces (GUI).

2.2 Image Acquisition by Using Opto-mechanical Apparatus

2.2.1 Coordinate for Images and Line Scan Imager

The coordinate definition and data structure for raw image and calibrated image of radiometry and geometry are shown as Fig. 2-1. After performing edge detection and ROI extraction on calibrated image, we can get the chip image (graylevel) and the chip edge image (binary) for defects inspection. Their coordinate definition and data structure are schematically shown in Fig. 2-2.

The coordinate definition and optical layout of opto-mechanical apparatus are shown as Fig. 2-3. Line scan imager has to be installed that CCD #1 is located at bottom and CCD #2048 at upper.

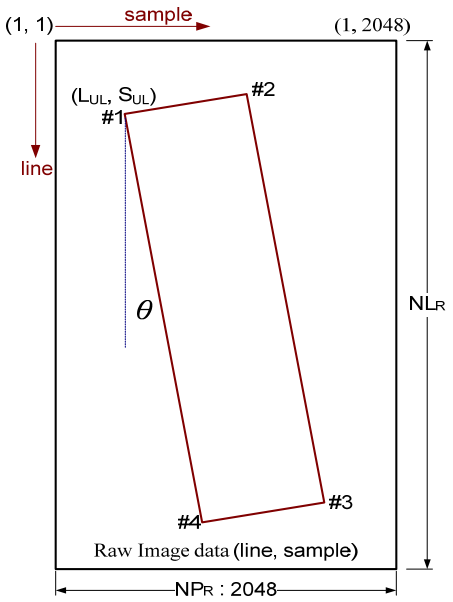


Figure 2-1. Coordinate and data structure of raw image.

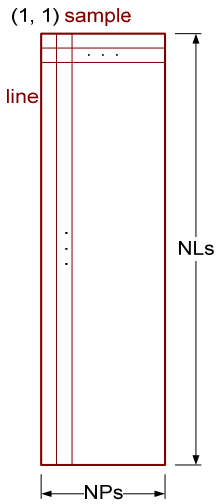


Figure 2-2. Coordinate and data structure of chip image.

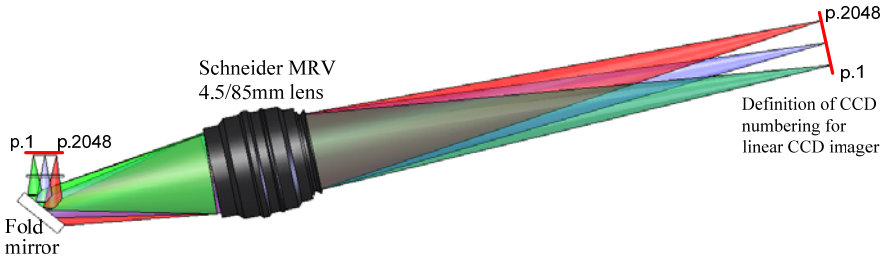


Figure 2-3. Coordinate definition and optical layout for OMA

2.2.2 Opto-mechanical Apparatus

According to results of system anlysis and design, a line scan imager of Basler sprint spL2048-140km [1] and a lens of Schneider MRV 4.5/85 [2] are selected to fit specifications of opto-mechanical apparatus. The imager has the maximum line rate of 140 kHz and the CCD size of 10 μm. The lens has the object spatial resolution of 5μm and magnification of 0.5 ~ 2. The variation of relative illumination and the geometry distortion of Schneider lens [2] is less than 3% and 0.2% respectively within its coverage of image height. Magnification of 2 is selected for OMA. Optical layout of OMA are shown in Fig. 2-3. A fold mirror is required for light tilt in OMA. Image acquisition card of DALSA/CORECO X64-CL Full [3] with maximum data transfer rate of 528 Mbytes/sec is selected.

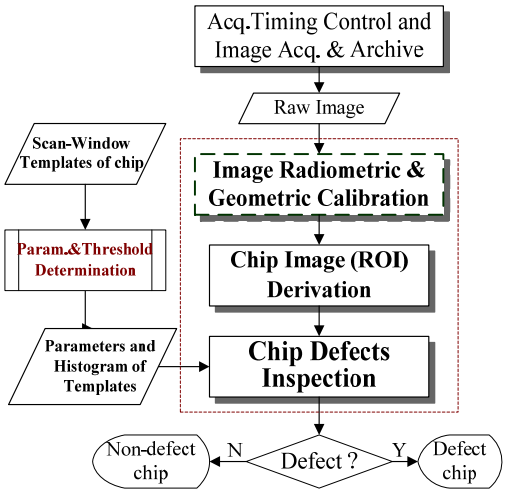
2.3 Illumination for Image Acquisition

The schematic structure of image acquisition region with illumination components is shown as Fig. 2-6. The spectrum, light source and lightening angle of illumination are also very important to acquire line images with good quality and contrast. Thus, we select LEDs of red spectrum for lighting. LED has advantages of small size, power efficient and modulation free. IEC is composed of an illumination module and a LED lighting controller.

3. Algorithms of Image Processing and Chip Defect Inspection

3.1 Image Processing for ROI Extraction

The flowchart of image processing and chip defect inspection for inspection system is shown in Fig. 3-1a. Before performing the chip defect inspection, acquired raw image has to be processed including image radiometric and geometric calibration, edge detection, affine transform parameters derivation, and image segmentation to derive chip images (ROI). Fig. 3-1b is the flowchart of ROI derivation.



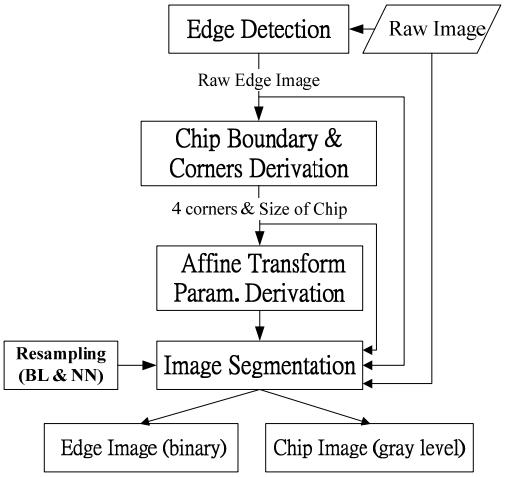


Figure 3-1a.(left) Flowchart of image processing and chip defect inspection

Figure 3-1b.(right) Flowchart of ROI (i.e. chip image) derivation

We can neglect the radiometric and geometric calibration for raw image to reduce processing time substantially based on good performance of selected Schneider MRV 4.5/85 lens and line scan imager of Basler sprint spL2048, and chips are located at about central region of lens. Algorithm of ROI derivation is described as follows:

(1) Edge detection: Canny edge detection [4] [5] is adopted for chip edge designation according to results of experiment using variant edge detection methods [6] [7]. Then we can derive the raw edge image with binary pixels, "1" representing edge and "0" non-edge pixels.

(2) Boundary and corners derivation for chip: Connect component of 8-neighbors is used to find chip edge on raw edge image. And 4 boundaries of chip can be found by method of least square linear fitting as well. The location of chip 4 corners then can be calculated according to 4 boundary lines of chip, shown in Fig. 2-1.

(3) Parameters derivation of Affine Transformation: Rotation angle (Θ) of chip can be derived by equation (3-1).

$$\theta = \tan^{-1}\left(\frac{Y_4 - Y_1}{X_4 - X_1}\right) \quad \cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots \text{(3-1)}$$

Where X_4, Y_4 and X_1, Y_1 represent lines and samples on raw edge image for corner #4 and #1 respectively. The location of corner #1, (X_1, Y_1), and Θ are the key parameters for affine transformation to derive chip images. Thus, we can have chip images, shown in Fig. 2-2 by equation (3-2).

$$\begin{aligned} X &= X' \cos\theta - Y' \sin\theta + X_1 \\ Y &= X' \sin\theta + Y' \cos\theta + Y_1 \end{aligned} \quad \cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots \text{(3-2)}$$

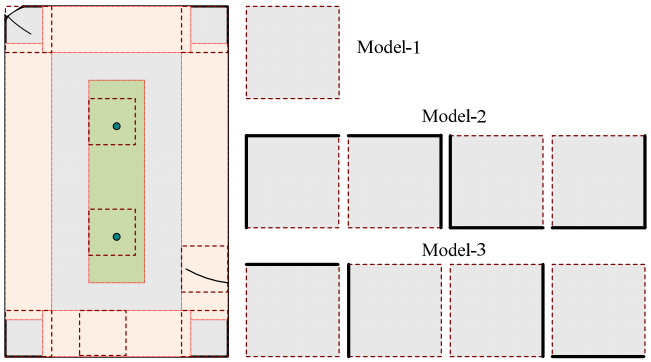
Where X' and Y' represent the location on coordinate of chip images. X and Y represent the location on coordinate of raw image.

(4) Image segmentation: After generating grid system of chip images, then we perform affine transformation based on Equation (3-2) to get all pixels value on chip images. Image resampling methods of Nearest Neighbor (NN) and Bilinear (BL) interpolation [8] are adopted for segmentating chip edge image and chip image respectively.

3.2 Scheme for Chip Defect Inspection

Fig. 3-2 is the schematic diagram of scan window for defect inspection. There're 3 modes of scan window for defect inspection, including Mode-1 for residual glue, Mode-2 for chipping and Mode-3 for crack. The size of scan window is determined according to the defects size range of inspected chips. In this study, the size of scan window is set as 21 x 21 pixels (about 100 μm), but can be changed depending on chip quality.

We first have to set the templates for edge image as the basis of inspection. Templates of 3 defect modes and schematic defect distribution in a scan window is shown as the upper diagrams in Fig. 3-3.



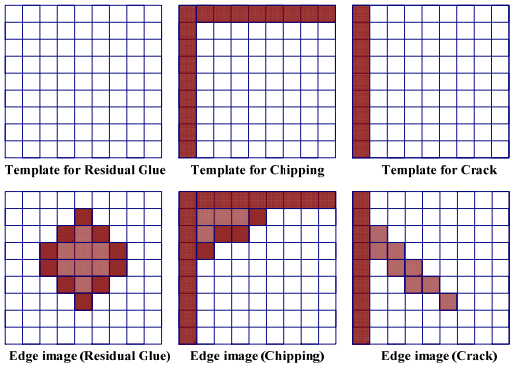


Figure 3-2.(left) Schematic diagram of scan window for defect inspection

Figure 3-3.(right) Templates of 3 defect modes and defect pixels distribution in a scan window

Mode-1, mode-2 and mode-3 of defects occur in the central, corner and peripheral region of chip respectively. Therefore, our algorithm can only handle them according to regions of their possible occurrence. The flowchart for chip defect inspection is shown as Fig. 3.4.

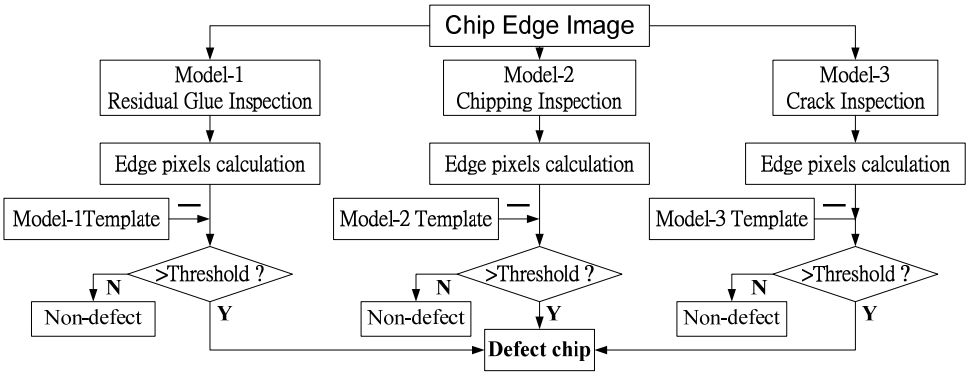


Figure 3-4. Flowchart of chip defect inspection

We check if there're defects within a chip in sequence based on 3 modes of scan window. Then chip defect inspection is conducted based on the flowchart of chip defect inspection and described as follows: (1) Calculate the edge pixels in a scan window based on a chip edge image in sequence within regions of possible occurrence for each defect mode, (2) Perform the subtraction of edge pixels between scan window of edge image and edge templates to derive the size of chip defect, (3) Check the result of subtraction if size of defect is greater than the criterion of impacting quality.

4. Experiments and Verifications

4.1 Experimental Material

Chip defect inspection system development is now in the phase of system integration and test. We generate some simulated raw images to verify proposed algorithms of the image processing for ROI derivation and the chip defect inspection preliminarily. Parts of these simulated raw images are shown in left diagrams of Fig. 4-1, 4-2 and 4-3.

4.2 Results and Discussion

We found Canny edge detection is the most suitable method from experimental results of edge detection. So we conduct Canny edge detection on all raw images to conduce to good edge extraction for defect inspection. And raw edge images and chip edge images with good detection results are shown in central and right diagrams of Fig. 4-1, 4-2 and 4-3 respectively. From results of edge detection and edge image extraction, edge of inspected chips with various inclination angles can be detected and chip edge image can be segmented precisely.

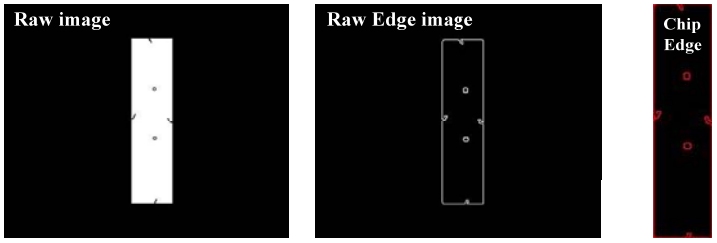


Figure 4-1. Edge detection and edge image extraction for chips without inclination

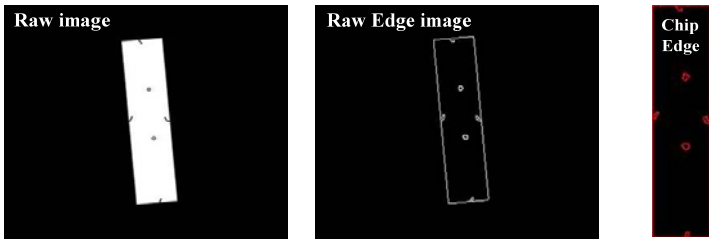


Figure 4-2. Edge detection and edge image extraction for chips with inclination of 5 degrees

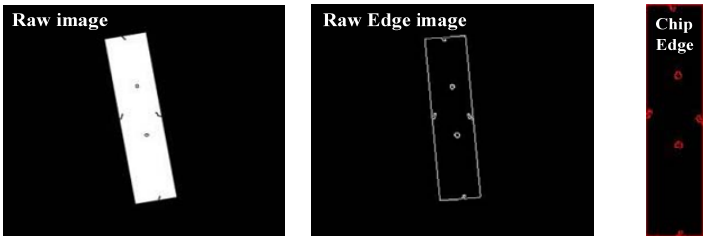


Figure 4-3. Edge detection and edge image extraction for chips with inclination of 10 degrees

Process of defect inspection within a chip is performed in sequence based on 3 modes of scan window after completing the ROI derivation process. We preliminarily verify defects with size of greater than 15 μm and their modes can be inspected correctly according to inspected results shown in Fig. 4-4.

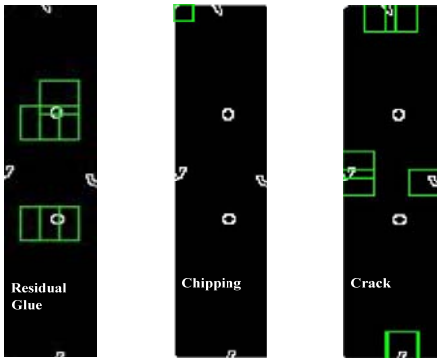


Figure 4-4. Results of defect inspection for chips with residual glue, chipping and crack

5. Conclusion

Proposed chip defect inspection system is mainly composed of an opto-mechanical image acquisition apparatus with high performance line scan imager, an illumination module and a software module of image processing and defect inspection. Novel algorithms of image processing and defect inspection for chips are described in detail in this article. Method of Canny edge detection is determined for the extraction of chip images with good performance. Algorithms are proved to be available and efficient for image processing and inspecting out the defects with size of greater than criterion.

Comparing with existent system, proposed chip defect inspection system using line scan imager with high performance has advantages that (1) chip images can be acquired under transporting process with constant speed for quick image acquistion and image processing, (2) only one raw image is acquired for each inspected chip, (3) efficiency of image processing and defect inspection can be improved significantly, (4) chips defect can be inspected automatically during packing process, and (5) a lot of manpower and cost for chip quality check can be saved for manufacturing.

Inspection system development is now in the phase of system integration and test. We'll conduct systematic tests to verify the functional and performance specifications of CDIS in near future. Our target is to provide an automatical defect inspection system to achieve the quality check of chips precisely on production lines.

Reference

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